Amendments to the Specification:

Please replace the paragraph beginning on page 3, line 14 with the following amended paragraph:

The address sequence for an interleave mode with a starting column address of "0 1 0 1" is as follows:

"0 1 0 1" (starting column address)
"0 1 0 0"
"0 1 1 1"
"0 1 1 0"
"[[0 0 0 1]]1 0 0 1"
"[[0 0 0 0]]1 0 0 0"
"[[0 0 1 1]]1 0 1 1"
"[[0 0 1 0]]1 0 1 0"

Please replace the paragraph beginning on page 3, line 24 with the following amended paragraph:

The address sequence for a serial mode with a starting column address of "0 1 1 0" is as follows:

"0 1 1 0" (starting column address)
"0 1 1 1"
"[[0 0 0 0]]1 0 0 0"
"[[0 0 0 1']]1 0 0 1"
"[[0 0 1 0']]1 0 1 0"
"[[0 0 1 1']]1 0 1 1"
"[[0 1 0 0']]1 1 0 0"
"[[0 1 0 1]]1 1 0 1"

Please replace the two paragraphs beginning on page 6, line 14 with the following amended paragraphs:

Figure 1 is a block diagram of a memory device including a ~~bust~~burst mode counter according to one embodiment of the invention.

Figure 2 is a block diagram of a portion of a ~~bust~~burst mode counter usable in the memory device of Figure 1 according to one embodiment of the invention.

Please replace the paragraph beginning on page 6, line 24 with the following amended paragraph:

A memory device that may use a ~~bust~~burst mode counter according to one embodiment of the invention is shown in Figure 1. The memory device illustrated therein is a synchronous dynamic random access memory ("SDRAM") 10, although the invention can be embodied in other types of DRAMs, such as packetized DRAMs and RAMBUS DRAMs (RDRAMS"), as well as other types of memory devices, such as static random access memories ("SRAMs"). The SDRAM 10 includes an address register 12 that receives either a row address or a column address on an address bus 14. The address bus 14 is generally coupled to a memory controller (not shown in Figure 1). Typically, a row address is initially received by the address register 12 and applied to a row address multiplexer 18. The row address multiplexer 18 couples the row address to a number of components associated with either of two memory banks 20, 22 depending upon the state of a bank address bit forming part of the row address. Associated with each of the memory banks 20, 22 is a respective row address latch 26 which stores the row address, and a row decoder 28 which applies various signals to its respective array 20 or 22 as a function of the stored row address. The row address multiplexer 18 also couples row addresses to the row address latches 26 for the purpose of refreshing the memory cells in the arrays 20, 22. The row addresses are generated for refresh purposes by a refresh counter 30, which is controlled by a refresh controller 32.

Please replace the paragraph beginning on page 7, line 14 with the following amended paragraph:

After the row address has been applied to the address register 12 and stored in one of the row address latches 26, a column address is applied to the address register 12. The address

register 12 couples the column address to a column address latch 40. Depending on the operating mode of the SDRAM 10, the column address is used for either of two purposes. First, in a normal operating mode, the column address is coupled through a burst counter 42 to a column address buffer 44 to select a column of memory cells in one or both of the memory arrays 20, 22. Second, in a burst operating mode, the column address is coupled to the burst counter 42 and used as a starting column address ("SCA"). The ~~bust~~burst counter then generates a sequence of column addresses starting at the SCA, and applies the sequence of column addresses to the column address buffer 44. In either case, the column address buffer 44 applies a column address to a column decoder 48~~a,b~~ for each array 20, 22. The column decoders 48~~a,b~~ apply respective decoded column addresses to respective sense amplifiers and associated column circuitry 50, 52 for the respective arrays 20, 22.

Please replace the paragraph beginning on page 9, line 1 with the following amended paragraph:

One embodiment of a portion of the ~~bust~~burst counter 42, which is shown in Figure 2, includes a column address counter 100 and counter control circuit 104. The column address counter 100 and the counter control circuit 104 are shown in Figure 2 along with the column address buffer 44, column address decoders 48a,b, and memory arrays 20, 22 used in the SDRAM 10 of Figure 1. The operation of the burst counter 42 is based on the realization that the correct sequence of column addresses can be generated in the 2-bit prefetch serial mode by decrementing the column address counter whenever the LSB of the externally applied starting column address SCA<0> is a "1." The operation of the burst counter 42 is further based on the realization that the correct sequence of column addresses can be generated in the 2-bit prefetch interleave mode by decrementing the column address counter whenever the NLSB of the externally applied starting column address SCA<1> is a "1."

Returning, now, to Figure 2, the ~~bust~~burst counter 42 implements the above principle of operation by controlling the count direction of the column address counter 100 using the counter control circuit 104 based on an INTL signal and the two least significant bits SCA<0:1> of the externally applied starting column address SCA<N:0>. The INTL signal is active high in the interleave mode and inactive low in the serial mode. The column address counter 100 receives SCA<N:1>, *i.e.*, all but the LSB of the starting column address SCA<N:0>, from the column address latch 40 (Figure 1) or other circuit. The counter circuit 100 generates a sequence of multi-bit column addresses CA<N:1> responsive to a clock signal CLK. The first of these multi-bit column addresses CA<N:1> consists of all but the LSB of the starting column address SCA<N:0> that was initially applied to the counter 100. Thus, the LSB of the column addresses CA<N:1> corresponds to the NLSB of the starting column address SCA<N:0>.

Please replace the paragraph beginning on page 11, line 9 with the following amended paragraph:

One embodiment of the counter control circuit 104 is shown in Figure 3. The counter control circuit 104 generates an active "1" DEC signal at the output of a ~~NOR~~ NAND gate 120 whenever either of the inputs to the ~~NOR~~ NAND gate 120 is low. The first input to the ~~NOR~~ NAND gate 120 will be low whenever a ~~NOR~~ NAND gate 124 decodes a high LSB of the starting column address SCA<0> and a high output from an inverter 126, which occurs whenever INTL is low indicative of operation in the serial mode. The second input to the ~~NOR~~ NAND gate 120 will be low whenever another ~~NOR~~ NAND gate 128 decodes a high NLSB of the starting column address SCA<1> and an active high INTL signal indicative of operation in the interleave mode. Thus, the NAND gate 120 will generate an active high DEC signal whenever the LSB of the starting column address is "1" when operating in the serial mode or whenever the NLSB of the starting column address is "1" when operating in the interleave mode.

Please replace the paragraph beginning on page 9, line 13 with the following amended paragraph:

For example, in the serial mode using the above example of a starting column address of "[[0]]1 1 0 1" the correct sequence is:

"1 1 0 1" (starting column address)
"1 1 0 0"
"1 0 1 1"
"1 0 1 0"
"1 0 0 1"
"1 0 0 0"
"[[1 1 1 1]]0 1 1 1"
"[[1 1 1 0]]0 1 1 0"

Please replace the paragraph beginning on page 9, line 26 with the following amended paragraph:

In the interleave mode, the correct sequence of column addresses for a starting column address of "1 0 1 1" is as follows:

"1 0 1 1"
"1 0 1 0"
"1 0 0 1"
"1 0 0 0"
"[[1 1 1 1]]0 1 1 1"
"[[1 1 1 0]]0 1 1 0"
"[[1 1 0 1]]0 1 0 1"
"[[1 1 0 0]]0 1 0 0"

Please replace the paragraph beginning on page 10, line 10 with the following amended paragraph: